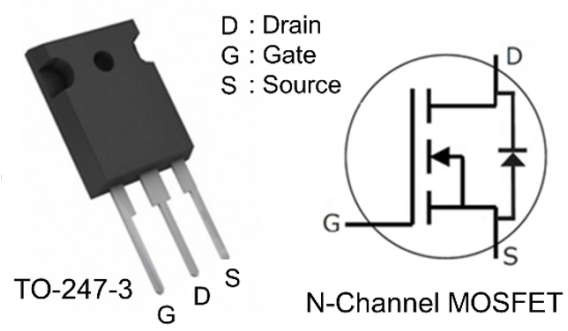
1200V 17mΩ SiC MOSFET

Features:

- High blocking voltage with low Rds(on)
- High frequency operation with low capacitance
- Simple to drive with -4V/+18V gate
- Robust body diode with low Qrr
- 100% avalanche tested



Benefits

- Superior robustness and system reliability
- Higher system efficiency
- Easier paralleling without thermal runaway
- Capable of high temperature application
- Faster and more efficient switching

Applications:

- EV/HEV charging station
- Energy storage and battery charging
- High voltage DC-DC converters
- Solar / Wind Inverters
- UPS and PFC

Key Performance and Package Parameters

Type	V_{DS}	$R_{DS(ON)}$	I_D@25°C	I_D@100°C	Marking	Package
PC017S120ANC	1200V	17mΩ	133A	94A	PC017S120ANC	TO247-3

Absolute Maximum Ratings(T_C =25°C unless otherwise specified)

Parameter	Symbols	Conditions	Value	Unit
Drain - source voltage	$V_{DS(max)}$	V_{GS}=0V, I_D=100μA	1200	V
Gate - source voltage	$V_{GS(max)}$	AC (f>1Hz, duty cycle<1%, pulse width<200ns)	-9 / +22	V
Gate – source voltage	$V_{GS(op)}$	static	-4 / +18	V
Continuous drain current (limited by $T_{J,max}$)	I_D	V_{GS} =18V, T_C=25°C V_{GS} =18V, T_C=100°C	133 94	A
Pulsed drain current	$I_{D(pulse)}$	T_C=25°C	267	A
Total power dissipation	P_D	T_C=25°C	625	W
Operating junction temperature	T_J		-55 to 175	°C
Storage temperature	T_{STG}		-55 to 175	°C
Soldering temperature	T_L		260	°C
Avalanche capability, single pulse*	I_{AV}	V_{DD}=100V, V_{GS}=10V, L=1mH	70	A
Avalanche capability, single pulse**	E_{AV}	V_{DD}=100V, V_{GS}=10V, L=1mH	2450	mJ

*100% tested in 60% rating
**100% tested in 36% rating

Electrical Characteristics at T_C= 25°C (unless otherwise specified)

Parameter	Symbols	Conditions	Value			Unit
			Min	Typ	Max	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=100μA	1200	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=20mA	2.2	3.0	4.2	V
		V_{DS}=V_{GS},I_D=20mA, T_J=150°C	-	2.3	-	
		V_{DS}=V_{GS},I_D=20mA, T_J=175°C	-	2.2	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=1200V, V_{GS}= 0V	0	0.5	100	uA
		V_{DS}=1200V, V_{GS}= 0V,T_J=175°C	0	5	200	
Gate-source leakage current	I_{GSS}	V_{GS}=18V, V_{DS}=0V	0	5	100	nA
Gate-source leakage current	I_{GSS}	V_{GS}=-4V, V_{DS}=0V	-100	-5	0	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=18V, I_D=50A	-	17	24	mΩ
		V_{GS}=18V, I_D=50A, T_J=175°C	-	33	-	
Transconductance	gfs	V_{DS}=20V, I_D=50A	-	41	-	S
		V_{DS}=20V, I_D=50A, T_J=175°C	-	39	-	S
Input capacitance	C_{iss}	V_{DS}=1000V, V_{GS}=0V f=100KHZ, V_{AC}=25mV	-	4350	-	pF
Output capacitance	C_{oss}		-	168	-	pF
Reverse transfer capacitance	C_{rss}		-	14	-	pF
Coss stored energy	E_{oss}		-	98	-	μJ
Turn-on switching energy	E_{ON}	V_{DS}=800V, V_{GS}= -4V/18V I_D=50A, $R_{G(ext)}$=2Ω, L=200μH	-	1481	-	μJ
Turn-off switching energy	E_{OFF}		-	330	-	μJ
Turn-on delay time	td(on)	V_{DS}=800V, V_{GS}=-4V/18V I_D=50A, $R_{G(ext)}$=2Ω, L=200μH	-	24	-	ns
Rise time	tr		-	25	-	ns
Turn-off delay time	td(off)		-	43	-	ns
Fall time	tf		-	9	-	ns
Total gate charge	Q_g	V_{DS}=800V, V_{GS}=-4V/18V I_D=50A	-	205	-	nC
Gate-source charge	Q_{gs}		-	53	-	nC
Gate-drain charge	Q_{gd}		-	76	-	nC
Internal gate input resistance	$R_{g(int)}$	f=1MHZ, I_D=0A	-	1.2	-	Ω

***Turn-off with -4V gate bias is highly recommended

Reverse Diode Characteristics at T_C= 25°C (unless otherwise specified)

Parameter	Symbols	Conditions	Value			Unit
			Min	Typ	Max	
Diode Forward Voltage	V_{SD}	V_{GS}=-4V, I_{SD}=40A,T_J=25°C	-	4.5	-	V
Diode Forward Voltage	V_{SD}	V_{GS}=-4V, I_{SD}=40A,T_J=175°C	-	4.0	-	V
Continuous diode forward current	Is	V_{GS}=-4V, T_J=25°C	-	100	-	A
Reverse recovery time	trr	V_{GS}=-4V, I_{SD}=50A,V_R=800V, $R_{G(ext)}$=10Ω, L=200μH dif/dt=2500A/us	-	35	-	ns
Reverse recovery charge	Q_{rr}		-	465	-	nC
Peak reverse recovery current	I_{rrm}		-	23	-	A

Thermal Characteristics

Parameter	Symbols	Conditions	Value			Unit
			Min	Typ	Max	
Thermal resistance	$R_{th(j-c)}$	Junction to case	-	0.20	0.24	°C/W

Typical Characteristics

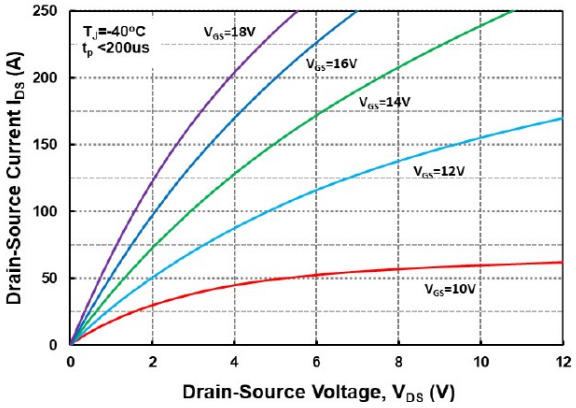


Figure 1: Output Characteristics,T_J=-40°C

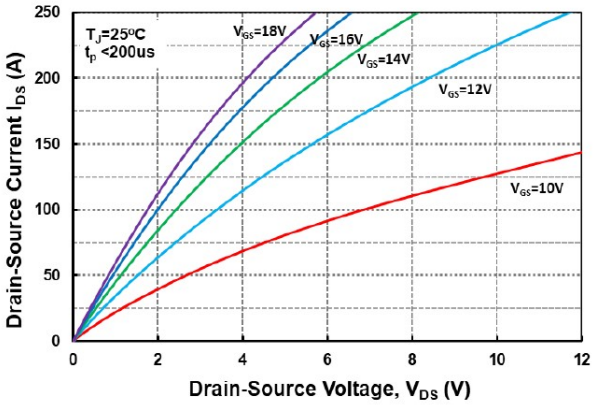


Figure 2: Output Characteristics, T_J=25°C

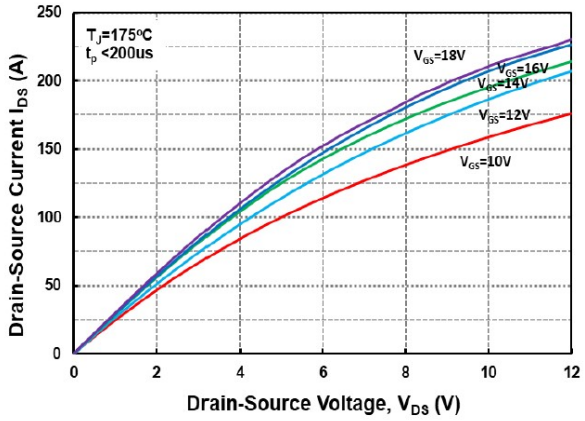


Figure 3: Output Characteristics,T_J=175°C

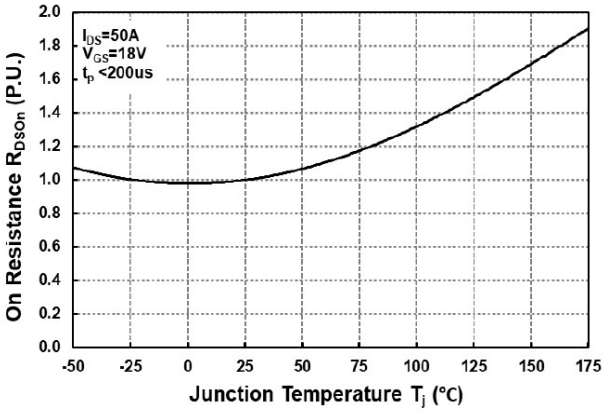


Figure 4: Normalized On-Resistance vs.Temperature

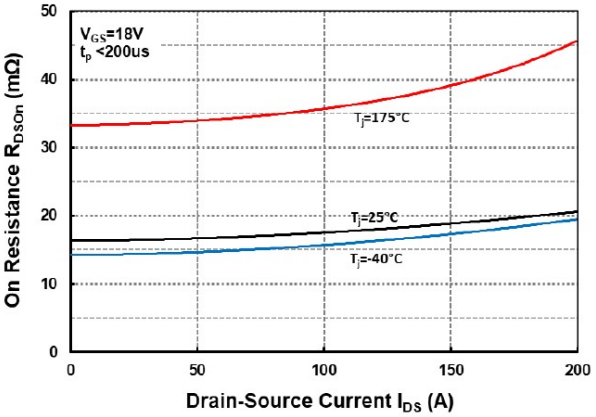


Figure 5: On-Resistance vs. Drain Current for Various Temperatures

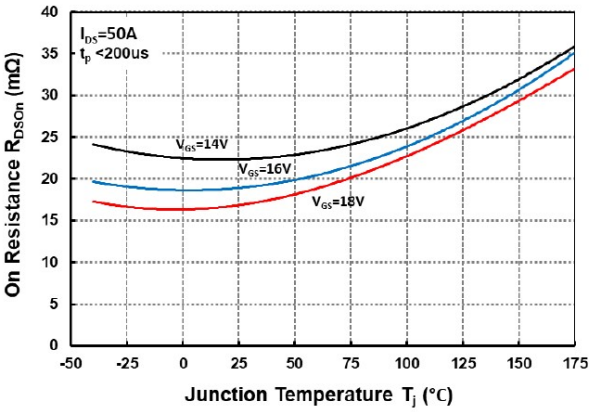


Figure 6: On-Resistance vs.Temperature for Various Gate Voltage

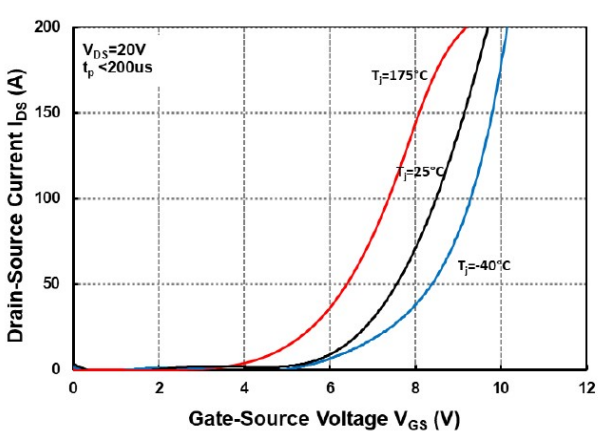


Figure 7: Transfer Characteristic for Various Junction Temperatures

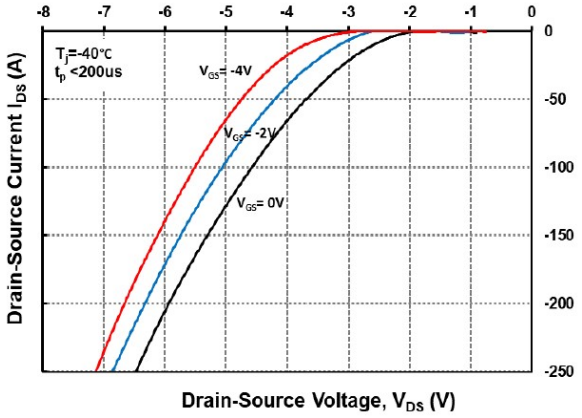


Figure 8: Body Diode Characteristics @ -40°C

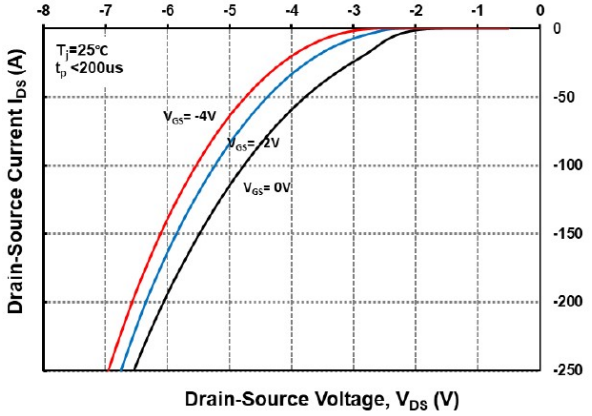


Figure 9: Body Diode Characteristics @ 25°C

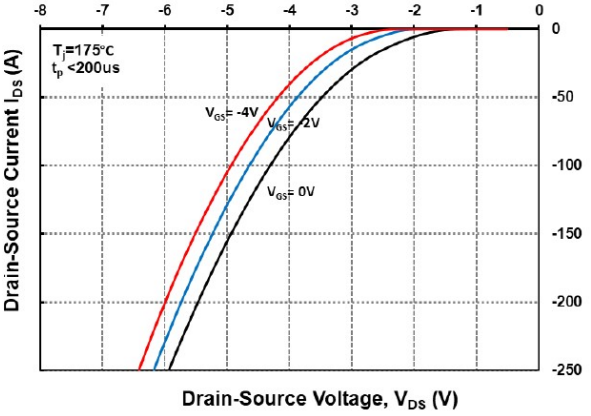


Figure 10: Body Diode Characteristics @ 175°C

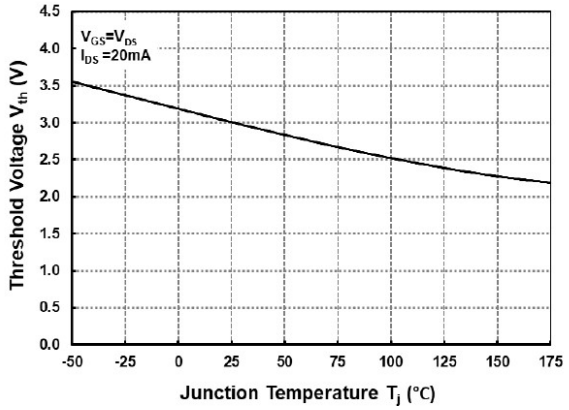


Figure 11: Threshold Voltage vs.Temperature

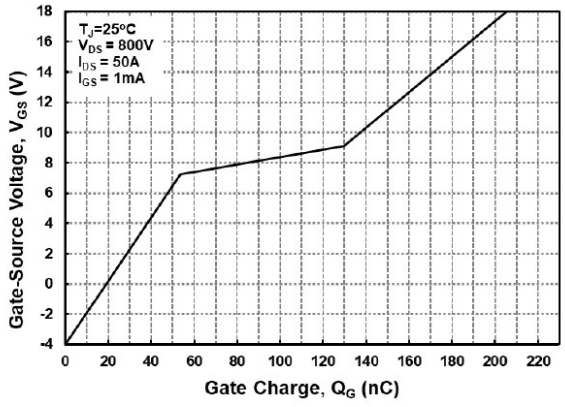


Figure 12: Gate Charge Characteristics

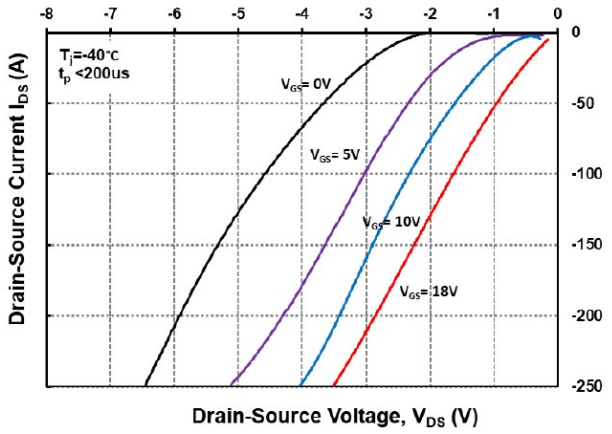


Figure 13: 3rd Quadrant Characteristics @ -40°C

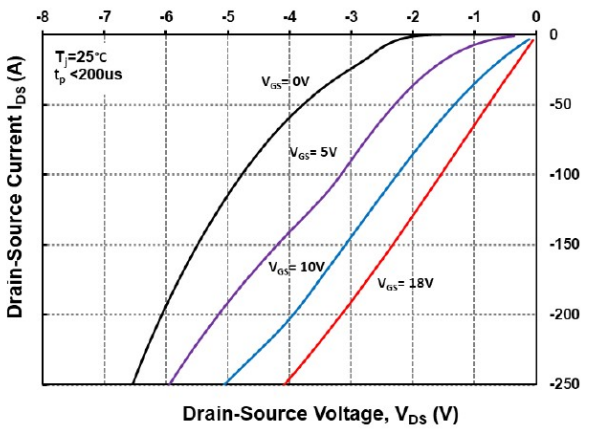


Figure 14: 3rd Quadrant Characteristics @ 25°C

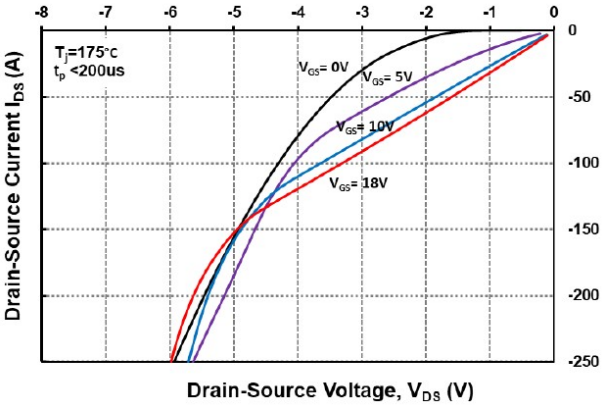


Figure 15: 3rd Quadrant Characteristics @175°C

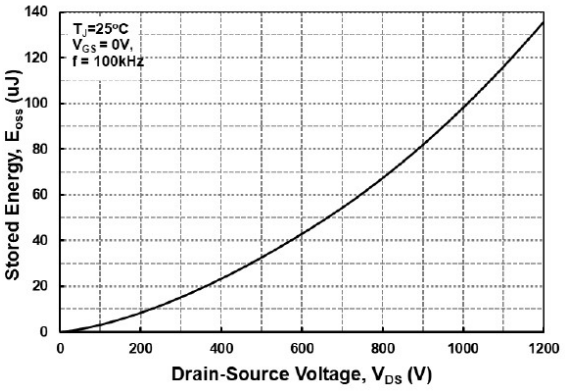


Figure 16: Output Capacitor Stored Energy

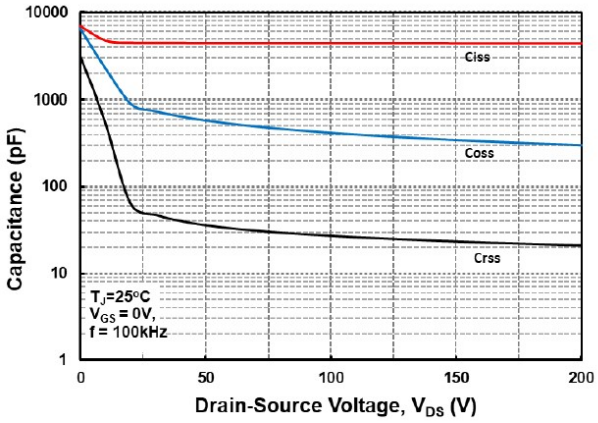


Figure 17: Capacitances vs. Drain-Source Voltage (0-200V)

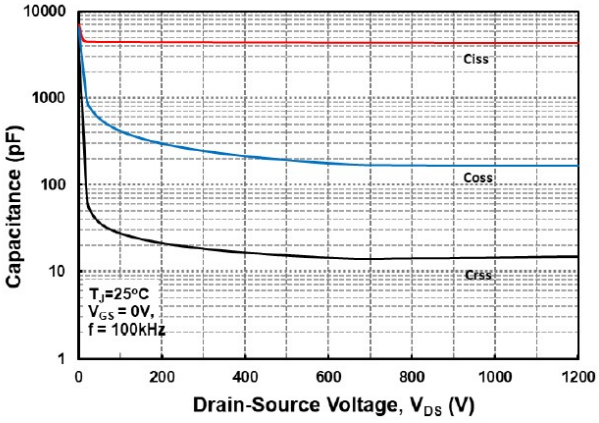


Figure 18: Capacitances vs. Drain-Source Voltage (0-1200V)

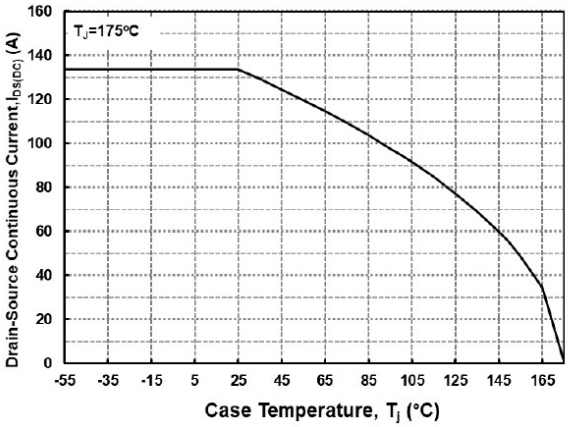


Figure 19: Continuous Drain Current Derating vs. Case Temperature

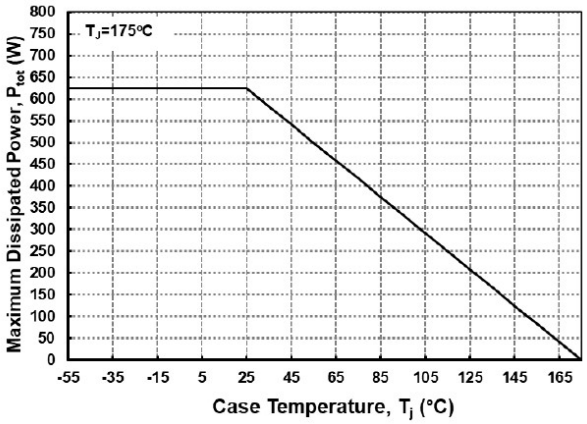


Figure 20: Maximum Power Dissipation Derating vs. Case Temperature

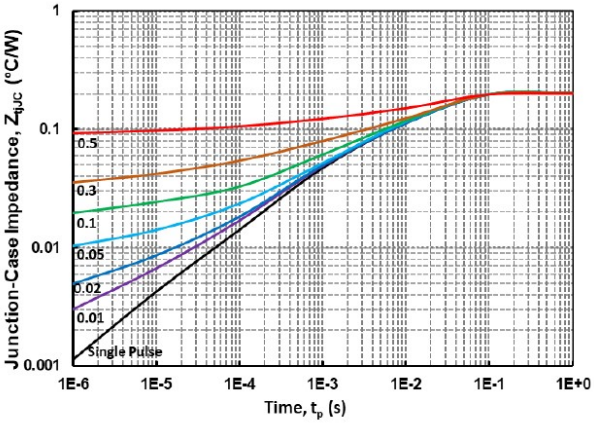


Figure 21: Transient Thermal Impedance (Junction – Case)

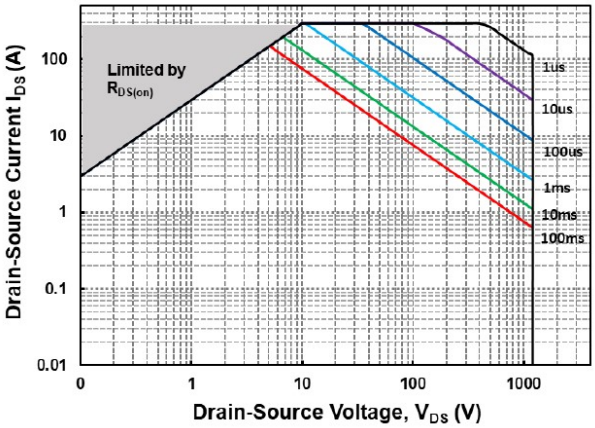


Figure 22: Safe Operating Area

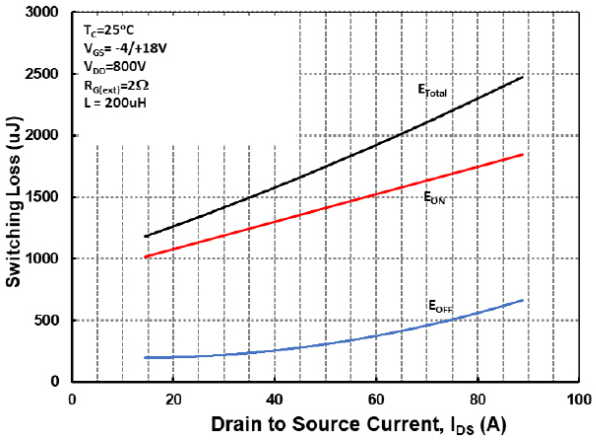


Figure 23: Clamped inductive Switching Energy vs Drain Current (V_{DD}= 800V)

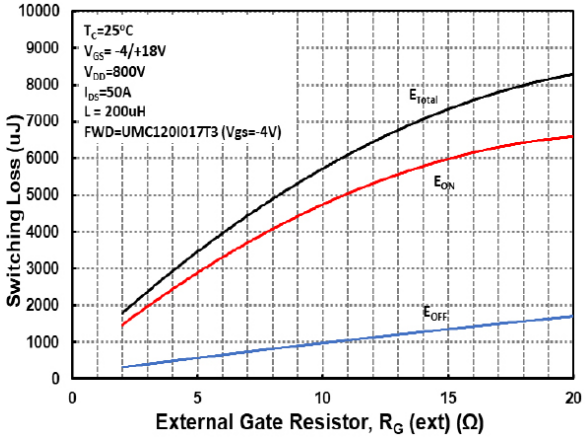


Figure 24: Clamped inductive Switching Energy vs External Gate Resistor $R_{G(ext)}$

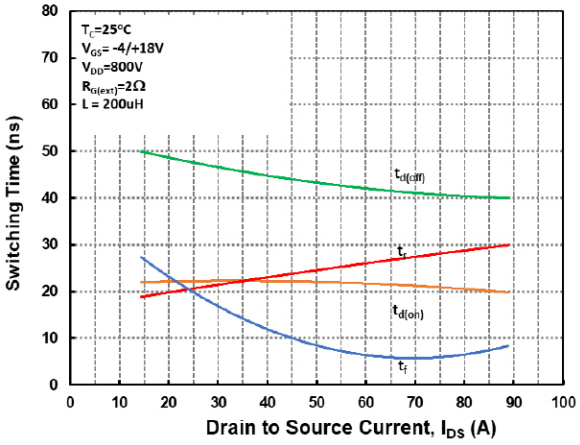


Figure 25: Switching Times vs Drain Current (VDD = 800V)

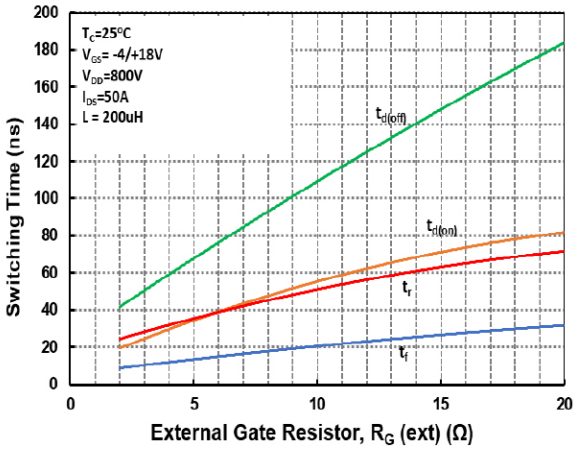
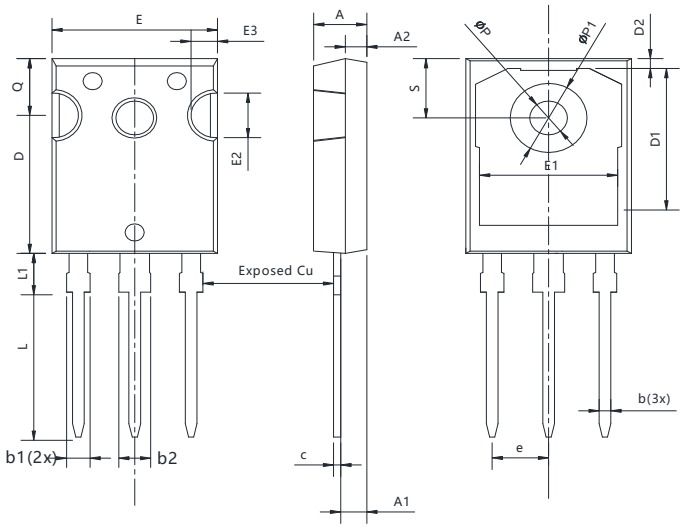


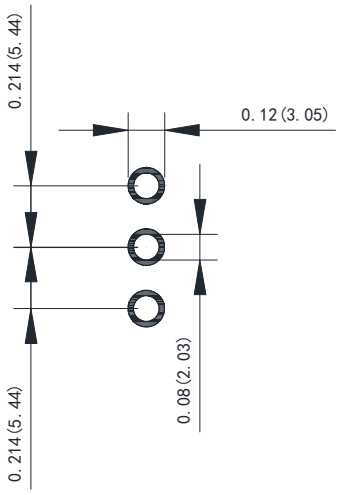
Figure 26: Switching Times vs External Gate Resistor $R_{G(ext)}$

Package Dimensions



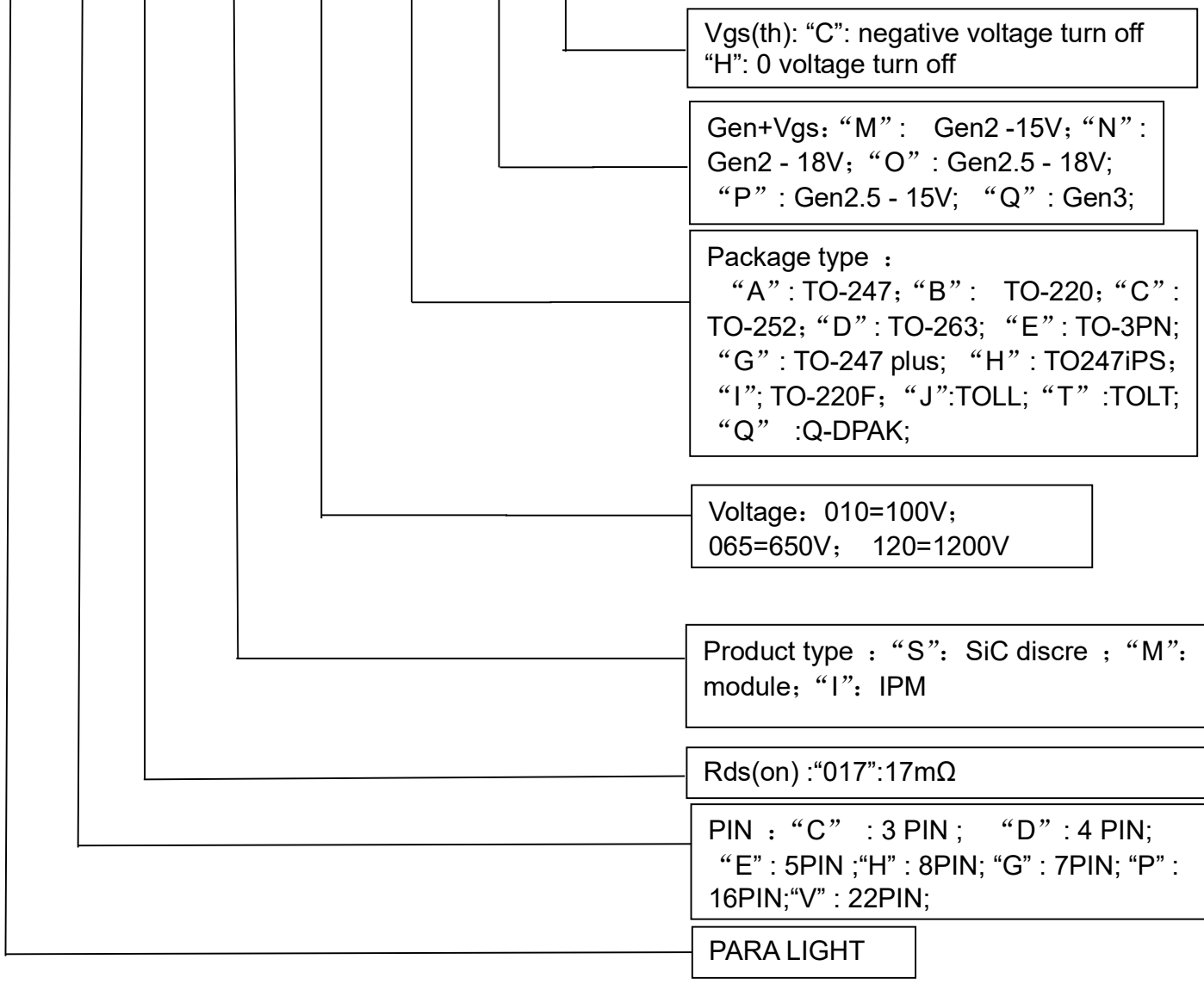
Common dimensions(mm)							
Symbol	**Min**	**Typ**	**Max**	**Symbol**	**Min**	**Typ**	**Max**
A	4.82	5.02	5.22	E1	13.01	13.26	13.51
A1	2.21	2.41	2.61	E2	4.71	4.91	5.11
A2	1.8	2.0	2.2	E3	2.26	2.46	2.66
b	0.95	1.2	1.45	e	5.44BSC		
b1	1.95	2.2	2.45	L	19.82	20.07	20.32
b2	2.95	3.2	3.45	L1	3.94	4.19	4.44
c	0.35	0.6	0.85	P	3.41	3.61	3.81
D	20.75	20.95	21.15	P1	6.94	7.19	7.44
D1	16.3	16.55	16.8	Q	5.59	5.79	5.99
D2	0.99	1.19	1.39	S	5.97	6.17	6.37
E	15.74	15.94	16.14				

Recommended Solder Pad Layout



PART NO. SYSTEM :

P C 017 S 120 A N C



Revision history

Document revision history

Date	Version	Changes
2026.03.12	A / 0	First release.